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PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application Number	10/065,016
		Filing Date	September 12, 2002
		First Named Inventor	Olivier Boireau
		Group Art Unit	2841
		Examiner Name	Lourdes C. Cruz
Total Number of Pages in This Submission	12	Attorney Docket Number	71522-2

ENCLOSURES (check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an Application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input checked="" type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Additional Enclosure(s) (please identify below): Declaration in Support of Petition <div style="text-align: center;"> FAX RECEIVED MAR 17 2003 TECHNOLOGY CENTER 2800 </div>
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	McGARRY BAIR LLP
Signature	Joel E. Bair, Reg. No. 33,356
Date	17 March 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being forwarded to Examiner Lourdes Cruz via facsimile sent to 703-872-9318 on March 17, 2003.

Typed or printed name	Andrea R. Wolters
Signature	March 17 2003

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G0088903

PTO/SB/17 (01-03)

Approved for use through 04/30/2003. OMB 0851-0032

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FEE TRANSMITTAL

for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 130.00)

Complete if Known

Application Number 10/065,016
 Filing Date September 12, 2002
 First Named Inventor Olivier Boireau
 Examiner Name Lourdes C. Cruz
 Art Unit
 Attorney Docket No. 71522-2

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MAR 17 2003

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None
☒ Deposit Account:

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Deposit Account Name McGarry Bair PC

The Commissioner is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments
☐ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 750	2001 375	Utility filing fee	
1002 330	2002 165	Design filing fee	
1003 520	2003 260	Plant filing fee	
1004 750	2004 375	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	

SUBTOTAL (1) (\$ 0)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent Claims	- 20 = 0	X	\$0
Multiple Dependent	- 3 = 0	X	\$0

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 18	2202 9	Claims in excess of 20
1201 84	2201 42	Independent claims in excess of 3
1203 280	2203 140	Multiple dependent claim, if not paid
1204 84	2204 42	** Reissue independent claims over original patent
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 0)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Small Entity

Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	2053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for ex parte reexamination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 410	2252 205	Extension for reply within second month	
1253 930	2253 465	Extension for reply within third month	
1254 1,450	2254 725	Extension for reply within fourth month	
1255 1,970	2255 985	Extension for reply within fifth month	
1401 320	2401 160	Notice of Appeal	
1402 320	2402 160	Filing a brief in support of an appeal	
1403 280	2403 140	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,300	2453 650	Petition to revive - unintentional	
1501 1,300	2501 650	Utility issue fee (or reissue)	
1502 470	2502 235	Design issue fee	
1503 630	2503 315	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	130
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1808 180	1808 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (times number of properties)	
1809 750	2809 375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 750	2810 375	For each additional invention to be examined (37 CFR 1.129(b))	
1801 750	2801 375	Request for Continued Examination (RCE)	
1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 130.00)

SUBMITTED BY

Name (Print/Type) Joel E Bair
 Signature *Joel E Bair*

Registration No. 33,356
 (Attorney/Agent)

(Complete if applicable)

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Date 17 March 2003

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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PATENT**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Olivier Boireau

For: INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD
ARRANGEMENT

Serial No.: 10/065,016


Examiner: Lourdes C. Cruz

Filed: September 12, 2002

Group Art Unit: 2841

Atty. Docket: 71522-2

Confirmation No.: 5731

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))	
I hereby certify that this correspondence is, on the date shown below, being:	
<input type="checkbox"/> deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents, Washington, DC 20231.	<input checked="" type="checkbox"/> transmitted by facsimile to the Patent and Trademark Office, to Examiner Lourdes C. Cruz at 703-872-9318.
Date: March 17 2003	Signature:  Andrea R. Wolters (type or print name of person certifying)

FAX RECEIVED

Commissioner for Patents
Washington, D.C. 20231

MAR 17 2003

TECHNOLOGY CENTER 2800

Sir:

PETITION TO MAKE SPECIAL

Pursuant to 37 CFR §1.102(d), Applicant hereby petitions the Commissioner to make the above-referenced application, Serial No. 10/065,016, special for the reason that an infringing device is presently being made, offered for sale, sold, or used in the United States. This petition is accompanied by the requisite statement in support hereof, and the fee set forth in 37 CFR §1.17(h).

The references most closely related to the subject matter of the claims are U.S. Patent No. 4,994,902 to Okahashi et al. and U.S. Patent No. 5,923,540 to Asada et al. Copies are attached. The U.K. Patent Office cited these references during examination of the priority application in the U.K., which application has claims substantially similar in scope to those of the present application.

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Art Unit: 2841

Okahashi '902 discloses a random set of pin locations (as illustrated in FIG. 6 and FIG. 7) for ground and power supply pins. There is no disclosure of inner portions and outer portions of an integrated circuit package. If it were to be interpreted by a person having ordinary skill in the art that the three rows and columns may be understood to comprise an outer portion, a middle portion and an inner portion, it is noted that one clock signal is located on an outer portion (outside row/column) and one clock signal located on a middle portion (of three rows/columns). The focus of Okahashi '902 is to link layers of multi-layer packages by arranging similar contacts/ pins to coincide vertically to higher layers, and is not remotely concerned with the difficulty in routing paths to/from the printed circuit board to the respective IC pins.

Okahashi '902 discloses a random distribution of power supply contacts, with (only by chance and not design) a minority of power supply contacts being located on an extremity of the IC. Thus, Okahashi '902 fails to disclose a majority of power supply contacts on an extremity of an integrated circuit package or printed circuit board. The feature of providing a majority of power supply contacts being located on an extremity in the present invention provides the advantage of enabling de-coupling capacitors to be located as close as possible to the power supply contacts. This minimizes track length and therefore resistance to the power supply contact, as described at paragraph 26 of the specification.

Furthermore, Okahashi '902 discloses one clock pin on an outer row/column and one clock pin on a middle row/column. However, it is noteworthy that the patent teaches, at col. 2 lines 44-45, that the clock signals can appear anywhere (so long as they are substantially matched on other 'vertical' layers for the co-processor!) But, regarding clock signals, one ordinarily skilled in the art is only taught by Okahashi '902 to surround clock signals by V_{ss} or V_{cc} fixed potential signals to keep them away from data (variable potential) signals. "This arrangement causes the fixed potential pins to shield electromagnetically the surroundings of the clock signal". Thus, Okahashi '902 fails to disclose a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board provides the advantage of enabling clock generation components to be located as close as

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possible to the IC's clock contacts, as described at paragraph 25 of the specification. This minimizes track length, and therefore undesired parasitic capacitance and resistance, to the clock contact pins, as described at paragraph 27 of the specification.

Furthermore, Okahashi '902 discloses data contact points along one side of an IC, but specifically being arranged distal from the clock contact points. Thus, Okahashi '902 fails to disclose a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board provides the advantage of allowing relatively easy access in routing paths to/from the data points, as described at paragraph 35 of the specification.

Asada '540 discloses all power supply contacts randomly located on the outside of ground contact points. Indeed, the location of the power supply contact in FIG. 9B is the same as FIG. 1 (see col. 9 line 63 to col. 10 line 3) and is therefore NOT on the extremity. Thus, Asada '540 fails to disclose a majority of power supply contacts on an extremity of an integrated circuit package or printed circuit board. As mentioned above, the feature of providing a majority of power supply contacts being located on an extremity provides the advantage of enabling de-coupling capacitors to be located as close as possible to the power supply contacts. This minimizes track length and therefore resistance to the power supply contact, as described at paragraph 26 of the specification.

Furthermore, Asada '540 discloses nothing about specific locations of clock signal pins, save that pins generally can be located outside and/or inside a set of ground contact points. Thus, Asada '540 does not disclose a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board provides the advantage of enabling clock generation components to be located as close as possible to the IC's clock contacts, as described on page 13 line 23-29 of the specification. This minimizes track length, and therefore undesired parasitic capacitance and resistance, to the clock contact pins, as described at paragraph 25 of the specification.

Furthermore Asada '540 discloses nothing about specific locations of clock signal pins, save that the pins generally can be located outside and/or inside a set of ground

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contact points. Thus, Asada '540 fails to disclose a majority of data signal contacts on an inner side of an outer portion of an integrated circuit package or printed circuit board. As mentioned above, the feature of providing a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board provides the advantage of allowing relatively easy access in routing paths to/from the data points, as described at paragraph 35 of the specification.

Respectfully submitted,
Olivier Boireau

Dated: 17 March 2003

By: 

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